

# RXT-6802

## Advanced 800G Multi-service Test Module

800GE IEEE  
800GE ETC  
800G PCS/FEC Testing  
2x400GE Testing  
8x100GE Testing  
400GE to 1GE Testing



True All-in-One, from 1.5M to 800G  
Dual test ports for all interfaces  
Up to four independent tests  
Best-in-class intelligent cooling system

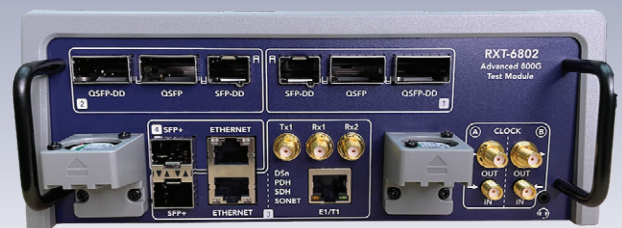
NEW

## for RXT-1202 Modular Test Platform



## Advanced 2x 800G/400G Multi-service handheld test set for Lab to Field Applications

VeEX® RXT is the industry's most flexible, compact, and future-proof handheld test solution for Core, Metro, Datacenter, and Access applications. The RXT-6800 800G/Dual 400G offers the flexibility of testing current interfaces and supporting future expandability for applications including Transport, Aggregation, cross-connect, 5G x-haul, and NEMs field support.



## Module Highlights

- 2x QSFP-DD800 test ports
- Supports pluggable client and line side DCO transceivers including QSFP-DD800, QSFP112, QSFP-DD, QSFP56 & QSFP28
- 800G to 100G Ethernet applications
- FEC and BER signal integrity testing
- PAM4 and NRZ SerDes up to 112G
- Multi-user independent port operation
- Comprehensive I2C capabilities for transceiver qualification
- Comprehensive test automation including Python API

## Applications

- Transceiver validation
- Signal integrity testing
- Network equipment, systems, and IC development
- Network verification and service delivery
- R&D, system verification test, and carrier labs
- Production and manufacturing test
- Benchmarking

## General

The RXT-6802 is based on an advanced programmable native PAM4 FPGA design which provides best-in-class signal integrity and future proof hardware to support current and emerging testing applications.

## Test Ports

- 2x QSFP-DD800
- 2x QSFP-DD 400G
- 2x QSFP56 200G
- 2x QSFP28 100G
- 2x QSFP+ 40G
- 2x SFPDD 100G
- 2x SFP56 50G
- 2x SFP+ 10G/1G

## Test Ports and Interfaces

### QSFP-DD800 Port Specifications

- Supports pluggable QSFP-DD800, QSFP112, QSFP-DD, QSFP56 and QSFP28 modules, AOCs, and DACs
- Supports DCO, ZR and ZR+
- Up to 800 Gbps data rate
- SerDes Lane rates
  - 8x 106G PAM4 SerDes
  - 8x 53G PAM4 SerDes
  - 8x 26G NRZ SerDes
- QSFP-DD MSA Hardware Specification Rev 7.0
- OIF CMIS 5.2
- OIF 400ZR 2.0
- Supports transceivers up to 30 watts

### Module Configuration & Port Groups

- Provides 2x port groups per test module
- Each port group can be reserved by an independent user and operated independently
- Factory Hardware Module options include:
  - Module with dual port groups
  - Module with reduced port option and single port group only

### Test Ports

Interface	Standard	Total Simultaneous Tests per Module
800GE KP4 RS-FEC	IEEE & ETC 800GAUI-8 PAM4 (106G per lane)	2x
2x 400GE KP4 RS-FEC*	2x 400GAUI-4 PAM4 (106G per lane)	2x
8x 100GE KP4 RS-FEC*	8x 100GAUI-1 PAM4 (106G per lane)	2x
400GE KP4 RS-FEC	400GAUI-8 PAM4 (53G per lane)	2x
4x 100GE KP4 RS-FEC*	4x 100GAUI-2 PAM4 (53G per lane)	2x
100GE KR4 RS-FEC	CAUI-4 NRZ	2x
100GE	CAUI-4 NRZ	2x
L1 Unframed Lane BERT, PRBSQ and SSPRQ Test Patterns	106.25G PAM4 and 53.125 PAM4 and 26.5625G NRZ	2x

\*Planned in future software release

## Host Test Module Features

### Signal Integrity Settings

- Adjustable TX swing, pre-cursor, pre-cursor 2, and post-cursor
- Receiver auto-tune mode for best performance

### Transmit Clock Source

- Chassis Clock Sources, (reference platform datasheet):
  - Internal stratum 3, 1.544 MHz, 2.048 MHz, 10 MHz, BITS/1.544 Mbps, or SETS/2.048 Mbps
- Recovered: from the incoming signal
- External: 1.544 MHz, 2.048 MHz, or 10 MHz; SMA connector (input shared between ports)

### Line Frequency Offset Generation

- Line frequency offset generation  $\pm 150$  ppm in 0.1 ppm steps, affects all lanes
- Constant generation
- Ramp generation: min offset, max offset, step size, and step duration settings
- Instantaneous offset

### Line Frequency Measurement

- Displays measured transmit line frequency offset from external reference clock in both Hz and ppm
- User defined alarm threshold for external transmit reference clock offset measurements
- Provides line frequency measurements in Hz with offset in Hz and ppm.
- User defined alarm threshold for received line frequency measurements

## Host Multi-Lane Unframed BERT, PRBSQ & SSPRQ Pattern Testing

### Per Lane Unframed BERT Test Pattern Generation and Measurement

#### Rates

- PAM4: N x 106.25G, N x 53.125G
- NRZ: N x to 26.5625G

#### Patterns

- PAM4 patterns: SSPRQ, PRBS9Q, PRBS11Q, PRBS13Q, PRBS15Q, PRBS20Q, PRBS23Q, PRBS31Q normal and inverted
- 25G NRZ patterns: PRBS9, PRBS11, PRBS13, PRBS15, PRBS20, PRBS23, PRBS31 normal and inverted

#### Results

- Per lane loss of pattern sync, bit error count, average, and current error rate results

#### Error Insertion

- Bit error generation per lane; supports single and rate insertion

## Transceiver Test Applications\*

### Information Display

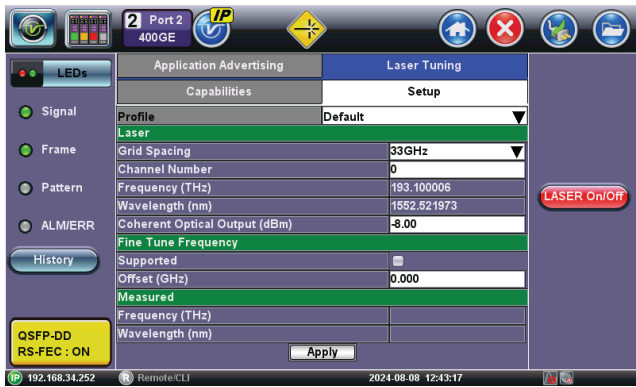
- Displays commonly used transceiver information saved in the I2C registers such as vendor name, part number, serial number, HW/FW revisions, power class, etc.

### QSFP-DD Application Advertising

- Provides the modules programmed capabilities
- Programs the modules internal settings

### Laser (ITLA) Tuning

- Grid spacing, channel number, frequency, wavelength
- Fine tuning offset
- Displays modules internally reported frequency and wavelength measurements
- Displays modules programmed capabilities



ZR Tuning Menu

### Coherent Optical Power

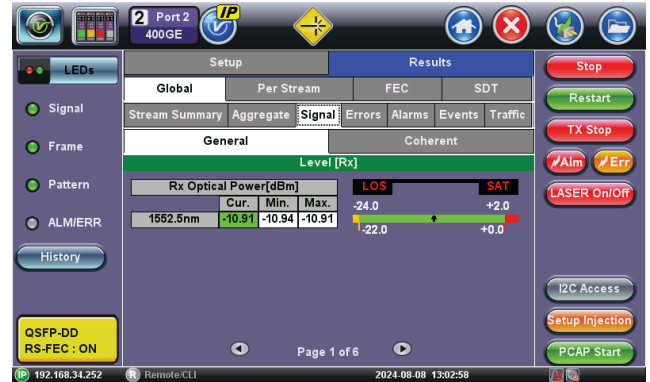
- Coherent optical power adjustment and measurement

### Optical Power

- Global and per optical lane power output enable/disable
- TX and RX per lane and broadband optical power level monitoring
- Current, min and max measurements
- Verifies transceiver internal or user defined thresholds for high alarm, high warning, low alarm, and low warning alarms



TX Power Level Settings



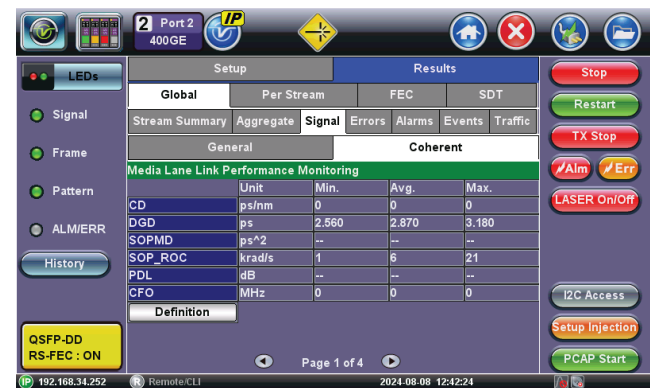
New TX Power Level in the Signal tab

### TX Bias Current

- Current, min and max measurements
- Verifies transceiver internal or user defined thresholds for high alarm, high warning, low alarm, and low warning alarms

### Coherent QSFP-DD C-CMIS Media and Host Performance Monitoring Stats (PM)

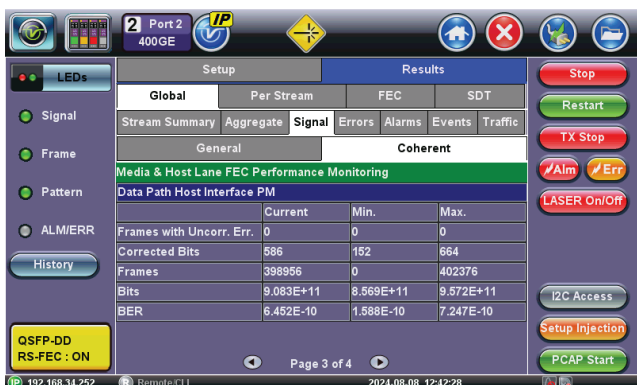
- Media Lane PM: Frames with Uncorrectable Errors, Corrected Bits, Frames, and Bits
- Data Path Host Interface PM: Frames with Uncorrectable Errors, Corrected Bits, Frames, and Bits
- Chromatic Dispersion
- Differential Group Delay
- Second Order Polarization Mode Dispersion
- State of Polarization Rate of Change
- Polarization Dependent Loss
- Carrier Frequency Offset
- OSNR
- eSNR
- Error Vector Magnitude
- TX Optical Power
- RX Optical Power
- RX Optical Signal Power
- Modulation Error Ratio



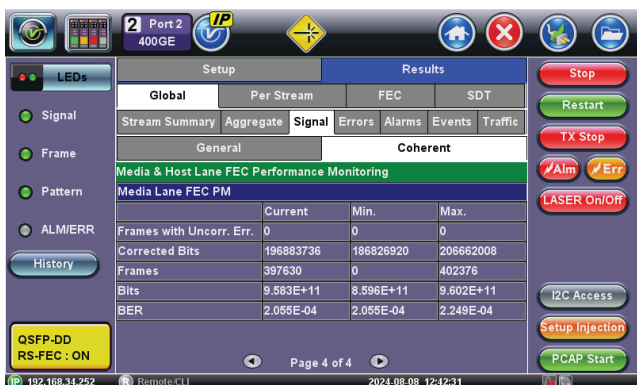
Coherent ZR+ Internal Media Lane Monitoring Statistics



Coherent ZR+ Internal Media Lane Monitoring Statistics



Data Path Host Interface FEC Performance Monitoring



Media Lane FEC Internal Performance Monitoring

### Temperature Monitoring

- Internal and cage temp monitoring
- Current, min and max measurements
- Verifies transceiver internal or user defined thresholds for high alarm, high warning, low alarm, and low warning alarms

### 3.3V Power

- Each port supports a variable 3.3V transceiver power supply to qualify transceiver specifications
- Provides host estimated current, min, and max transceiver power, voltage, and current measurements
- Displays the transceiver internal current, min, and max voltage measurements
- Verifies transceiver internal or user defined thresholds for high alarm, high warning, low alarm, and low warning alarms

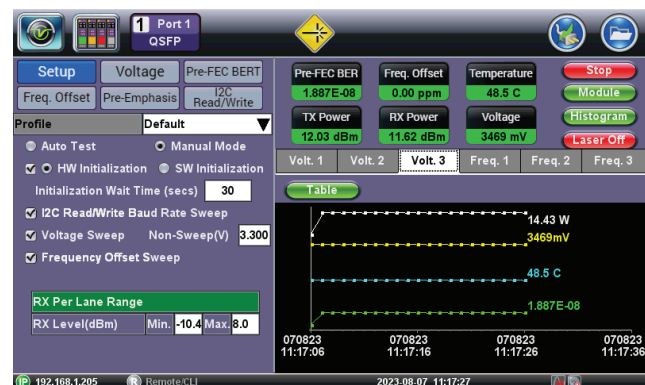
### I2C

- Complete I2C register read/write access

\*Note: Features are dependent on the installed pluggable transceiver.

### Advanced Optical Transceiver Test Suite

- Pre-FEC BER validation on a per-lane basis, over operational voltage and frequency offset range to verify optical module integrity before FEC is applied to the PAM4 signal.
- Pre-Framed BER (Lane BERT) validation for non PAM4 interfaces.
- Voltage, temperature, and Pre-FEC BER are monitored and displayed for the duration of the test. A histogram function clearly displays all three measurements for easy correlation and tracking of any abnormal changes.
- Pre-FEC BER and Optical Power threshold settings for PASS/FAIL indication.
- Pre-emphasis: Pre-taps, post-taps, and attenuation settings for PAM4 signal conditioning on the host side to help verify and stress transceiver tolerance and performance.
- Supply Voltage Tolerance Verification: Sweep range from 3.135V to 3.465V (3.300V +/- 5%) to verify compliance with optical transceiver MSA standard.
- Power Consumption Verification: Monitors the optical transceiver's power consumption (Watts), to verify conformance to its specified power class.
- Temperature Monitoring: QSFP-DD module and cage temperature monitoring with built-in shutdown protection of the optical module if the temperature increases beyond a certain high temperature.
- Frequency Tolerance Verification: Sweep range from -100 ppm to +100ppm (in 0.1ppm/step).
- I2C Baud Rate Sweep: QSFP-DD and OSFP sweep range 100K to 4000K. QSFP28 sweep range (20K to 1000K).



## Ethernet/IP

### Traffic Generation/Test Stream Flows

- Multiple independent test stream flows with separate rate, addressing and traffic parameters
- The test stream is generated with a signature field in the beginning of the payload area for traceability and measurement purposes
- 800/400GE (16 streams) and 100 (32 streams)
- L2, L3 or L4(UDP)
- IP Version: IPv4 or IPv6
- Frame sizes: 64 to 16,000 bytes; fixed, random, increment, or decrement generation
- Test Pattern: PRBS31 normal and inverted, 32-bit user
- VLAN tags up to 4 levels
- MPLS tags up to 4 levels
- Custom frame tags

### Traffic Rate Generation

- Full rate generation and analysis
- Constant, IPG, Ramp or Burst scheduling

### Flow Control

- Pause frame generation and response

### Error Generation

- Port based - Runt, FCS, IP Checksum, and UDP Checksum
- Per test stream - Payload Bit and Sequence
- Single and rate insertion

### Alarm Generation

- Remote and Local Fault alarms
- Auto reply to Local Fault option

### Benchmarking

- Throughput
- RFC 2544
- Y.1564

### Service Disruption Time (SDT) Measurement

- Min, max, and average measurement

### Loopback/Reflection Mode

- L2/L3

### Result Filtering

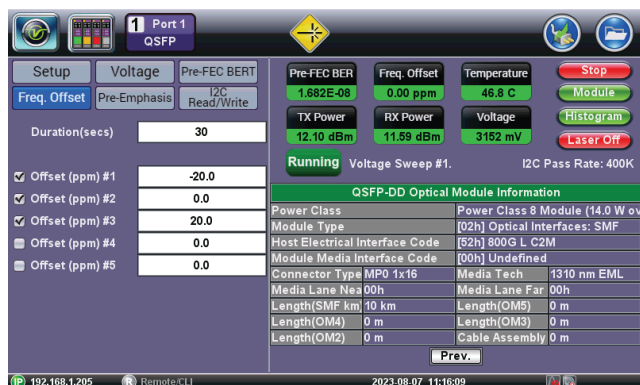
- Results can be filtered by up to 4 VLAN tag TPIDs

### Transmit and Receive Port Counts

- Packets, packets/second, bytes, Mbps, % BW
- VLAN packets, MPLS packets
- IPv4 and IPv6 packets
- L1 and L2 Statistics

### Receive Port Counts

- TCP, UDP, IGMP, ICMP packets
- Broadcast, multicast, unicast
- Jumbo, super jumbo packets (greater than 9216 bytes)



## PCS/FEC Layer

### PCS/FEC Lane Numbering

- Supports lane number swapping and rotation
- Displays received lane ID, lane # and channel assignments

### PCS/FEC Lane Skew

- Per lane static skew generation and measurement

### Error Generation

- FEC Correctable Symbol
- FEC Uncorrectable
- 256B/257B Transcode
- 64B/66B
- SYNC HDR, BIP8 (CAUI-4)
- Single and rate insertion

### Alarm Generation

- FEC LOA
- High SER
- FEC REM Degraded SER
- FEC Local SER Degraded
- FEC Alignment marker loss per lane (LOAMPS)
- HighBer, Block Lock, (CAUI-4)

### Error Results

- FEC Correctable Symbol with symbol error per codeword distribution
- FEC Uncorrectable
- 256B/257B Transcode
- 64B/66B
- SYNC HDR, Alignment Marker, BIP8 (CAUI-4)

### Alarm Results

- FEC LOA
- FEC High SER
- FEC Degraded SER
- FEC Remote Degraded SER
- FEC Local Degraded SER
- FEC Alignment marker loss per lane (LOAMPS)
- HighBer, Block Lock, (CAUI-4)

### Port Distribution Results

- VLAN distribution by tag level and quality of service level
- MPLS distribution by tag level and traffic class
- Frame size distribution for 64, 65-127, 128-255, 256-511, 512-1023, 1024-1518, 1519–max byte ranges with support for counts and percentage

### Port Utilization Counts

- Total, IPv4, IPv6, VLAN, MPLS binning
- Current, min, max, and average % BW, Mbps, and packets per second statistics for generated and received traffic
- L1 and L2 statistics

### Port Errors

- Runt, FCS, IP Checksum, UDP Checksum, and undersized
- Displays counts, errored seconds, current and average error rates

### Port Alarms

- Loss of Link, Local Fault, and Remote Fault

### Test Stream Results

- Independent set of results per test stream
- Transmitted and received frame counts, byte counts and rate
- Sequence errors, payload bit errors and lost frame counts in errored seconds, current and average rates
- Latency min, max, and average measurements
- Packet/frame jitter min, max, and average measurements
- L1 and L2 statistics

### Packet Capture

- Wire speed PCAP capture
- Full frame or packet slicing

## General Specifications

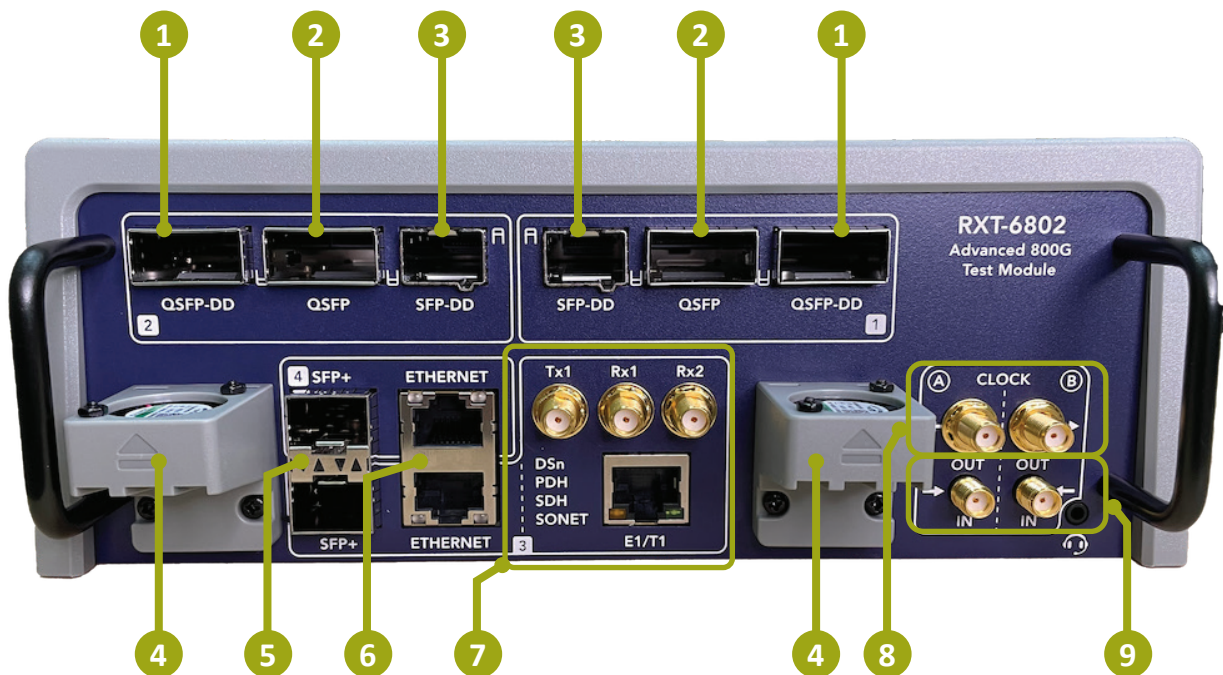
### Operating Temperature

- 5°C to 35°C (41°F to 95°F)

## General

Power Consumption		RXT-1202 Chassis	260 x 180 x 65 mm (10.2 x 7.1 x 2.6 in)
Maximum	300 Watts <sup>3</sup>	Test Set (combined)	260 x 200 x 108 mm (10.2 x 7.9 x 4.3 in)
Environmental		Weight	
Operating Temperature	5°C to 35°C (41°F to 95°F)	RXT-6802	1.73 kg (3.8 lb.)
Storage Temperature	-20 to 70°C (-4 to 158°F)	RXT-1202	1.32 kg (2.9 lb.)
Humidity	5% to 90% non-condensing	9-cell Li-ion battery	0.54 kg (1.2 lb.) <sup>5</sup>
Dimensions		Total (Test Set)	3.59 kg (7.9 lb)
RXT-6802 Module	208 x 155 x 77 mm (8.2 x 6.9 x 3.0 in)		

1. Basic web and cloud services available free of charge
2. Check with factory for specific module versions compatible with the new RXT-1202 platform
3. Requires RXT-1202 high-power platform and A01-00-019G 24VDC/12.5A AC/DC adapter.
4. Range specified up to 100G operation. For 400GE it is recommended to be operated below 32°C (90°F).
5. Requires B02-09-007G high-capacity 400G-ready battery pack.



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|---|---|
| <p><b>1</b> 800G QSFP-DD800 (800GBASE-X), 400G QSFP-DD (400GBASE-X, 400GZR/ZR+), QSFP56/QSFP28 (200G, 100G, 50G)</p> <p><b>2</b> QSFP+ (40G)</p> <p><b>3</b> SFP-DD56/SFP56/SFP28 (100G, 50G, 25G BASE-X)</p> <p><b>4</b> External QSFP-DD Cooling Fans. Cools exposed transceivers head (Field replaceable).</p> <p><b>5</b> 2x SFP+/SFP (10G, 1G BASE-X). Future use.</p> | <p><b>6</b> 2x RJ-45 (10/100/1000BASE-T)</p> <p><b>7</b> Coaxial SMA and RJ48 (future use)</p> <p><b>8</b> 2x Independent Reference Clock Outputs (future use)</p> <p><b>9</b> 2x Independent Reference Clock Inputs (future use)</p> |
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